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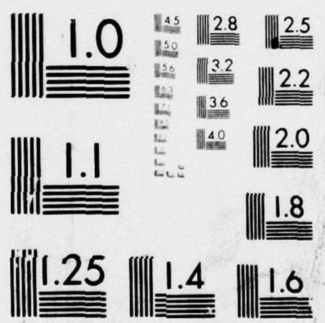

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NANOSECOND PULSERS FOR MM WAVE TUBES

J. STOVER, N. KOMATSU, A. NIETO
HUGHES AIRCRAFT COMPANY
GROUND SYSTEMS GROUP
FULLERTON, CA 92634

February 1980

Third Interim Report June 1979

Through September 1979

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VMOS FET
Marx Modulator
Bipolar Junction Transistor (BJT)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A pulser with turn on-turn off switching capability in the nanosecond region has been fabricated and is presently in the preliminary stage of evaluation. The unit is designed to deliver a 1000 V pulse into a 50 ohm resistive load.

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CONTENTS

LIST OF FIGURES

SUMMARY

The above pulser consists of a 10 stage Marx circuit to initiate the pulse, a 11 stage Marx circuit to terminate the pulse, coupled together by a 11 stage isolation circuit. Raytheon's RS3500 (formally, AVG) avalanche transistors are used throughout the Marx and coupling circuit.

The development of a high voltage probe, designated as Probe Prototype 1 (PP1), has been completed. The unit interfaces with the Tektronix S-3A sampling head (X100) to give an overall voltage division of 1000:1. The probe combination expands the maximum voltage capability of the S-3A to 2 KV. The S-3A/PP1 probe is presently being used in support of the nanosecond pulser design. Additionally, a probe (PP2) compatible with 50 ohm measurement systems has been designed, fabricated, and is now in test.

PROGRAM OBJECTIVES

As stated in the previous reports, the efforts of the program are directed toward the development of nanosecond pulsers for MM wave tubes. The specific goal is to fulfill the requirements of TASK A and TASK B (Technical Guidelines, 16 July 1979). Means to achieve the two goals will be through the implementation of the Marx circuit, using avalanche transistor RS 3500 as the switching element.

The possibility of replacing the avalanche transistor with VMOS FET's remains an open item. A recent evaluation of Siliconix VN120A VMOS FET with a 350V rating indicated the higher voltage device did not exhibit the favorable avalanche characteristics found in the lower 90V units (i.e., 2N6661). The evaluation will be continued as newer high voltage devices become available.

NANOSECOND PULSER DESIGN

SWITCHING DEVICE TEST

Tests have recently been initiated to determine the power handling capabilities under pulse condition of the RS3500 avalanche transistor. Tests will be made on a single device basis as well as on a series Marx type configuration. The increase in value of the capacitors in the Mark type circuitry, brought about by increased pulse width, necessitates these tests. The proposed test circuitry is shown in Figure 1. The device power dissipation can be altered by varying the value of capacitor, resistor and/or the pulse repetition rate.

The recent availability and ensuing purchase of the "K" type (RS 3501) packaged standard version of the RS 3500 in (TO-5 packages) will be tested to determine if an improvement in rise time can be achieved due to the RS3501 lead configuration.

A. Switch Module Development

Preliminary to the design of the circuitry required for TASK A and TASK B, the pulser shown in Figure 2 was designed, fabricated, and is presently being evaluated. The unit as shown delivers a negative output pulse of 1000V at 20 AMPS to a 50 ohm resistive load. With a minimal reconfiguration of the circuit, a positive output pulse can be realized.

The pulser consists of three major sections; 1) a Marx configuration in the forward direction to initiate the load current, 2) a similar Marx configuration to terminate the load current and 3) the isolation circuitry to prevent inadvertent interaction between the two Marx circuits.

The switching device used in all three sections of the pulser is a silicon avalanche transistor, RS3500 manufactured by the Raytheon Company in Mountain View, California.

Shown in Figure 3 are waveforms of the output pulse. Normal representation on the Tektronix 7904 oscilloscope screen of the waveforms using the S-3A sampling head, plug in, and sampling time base was not possible due to a malfunction of the S-3A head. The pictures shown were taken using a 50 ohm 6035 probe, 7A19 vertical plug in, and 7B53A horizontal time base unit. Such being the case, waveforms with a more exact rise time, free from the appearance of small oscillation could not be realized with the test equipment on hand.

Additional design effort is required on the circuit shown in Figure 2 to allow an increase of the pulse repetition rate of the pulser to the maximum of 20 KHz. The required circuit will be of the form shown in Figure 4 to actively charge the capacitors (4700 pf) in the Marx circuit in the maximum allowable time of approximately 40 μs.

B. Pulse Transformer Development

Several alternative designs have been considered in the development of subnanosecond high current, high voltage pulse transformers.

The initial design discussed in the last report, of using conductors of deposited copper on Kapton, was found inadequate due to poor coupling.

Another method considered was the cascade of several sections of bifilar wound transformer using litz wire wound on a small ferrite toroid, and connected in a transmission line configuration. Further efforts on the unit were terminated after several attempts of impedance matching the cascaded sections failed. This resulted in a large distortion to appear on the leading edge of the waveform.

Further work in this area has been suspended until the first quarter of 1980 due to funding.

C. Current Transformer Development

An extensive literature search was made to assess the state-of-the-art measurement of large amplitude current with subnanosecond rise time. Although several potentially feasible approaches for current measurement have been identified, each had one or more disadvantages ranging from construction difficulty to difficulty in calibration. One aspect the various methods all had in common was that each was custom designed for a specific application.

The actual development of a current transducer will be delayed until the first quarter of 1980. During the interim period, the Tektronix CT-1 current probe will be used. In the event a single CT-1 capacity is exceeded, two CT-1 will be installed to operate in parallel.

D. Voltage Divider Development

The capacitive divider probe discussed in the last report was found susceptible to high frequency oscillations. The probe design was modified to expand its capability to d-c measurements, and to reduce its oscillatory behavior. This new probe was also designed to interface with the Tektronix S-3A sampling head probe.

Measurements taken with the new probe, on a Mark modulator circuit, indicated an undesirable trade-off in rise time capability was necessary to eliminate spurious oscillatory behavior. These oscillations were found to be a function of the impedance match between the new probe and the S-3A X1 probe tip. The S-3A X1 probe tip has 100 K ohms input impedance. The probe had an attenuation ratio of 1000:1. It was found that if the S-3A X100 probe tip was used to interface with the new probe, the oscillations could be controlled. The S-3A X100 has a 1 megohm input impedance. The ratio of the new probe was reduced to 10:1 to maintain an overall 1000:1 attenuation ratio. This configuration was designated Probe Prototype 1 (PP1).

The equivalent circuit of PP1 is shown in Figure 5. Low frequency compensation was accomplished by adjusting C, R_c and R, while the high frequency response was adjusted through varying R_i, Z_B, R_c and R_o. Photographs of the completed probe can be seen in Figures 14, 15 and 16.

PP1 calibration was accomplished using the set-up shown in Figure 6. The low frequency and d-c calibration utilized a HP 214A pulser. Figures 7, 8, and 9 show the d-c response following a step input. Trace thickness variations are due to different vertical sensitivity settings. Figure 10 shows the PP1's low frequency (below 100 MHz equivalent bandwidth) response.

The Tektronix Model 109 reed pulser was the source for high frequency (fast rise time) calibration measurements. Figure 11 shows the Tektronix Model 109 as seen by the S-3A X100 probe. The rise time is 290 ps. This translates to an equivalent bandwidth of approximately 1.2 GHz. The PP1 was inserted between the Tektronix 109 and the S-3A X100 Probe. Figure 12 shows the resulting rise time of 300 ps. The probe only rise time is derived from

$$\sqrt{(t_{r\ system})^2 + (t_{r\ DUT*})^2} \cong t_{r\ observed}$$

which implies

$$t_{r\ PP1} \cong \sqrt{(t_{r\ obs})^2 - (t_{r\ system})^2}$$

$$\cong 77\ ps$$

*Device Under Test

Figure 13 illustrates the level of high frequency compensation and damping achieved.

Using the same general design philosophy used on PP1, a second probe has been designed. This Probe Prototype 2 (PP2) is to fill a requirement for a 2 kV fast voltage probe compatible with 50 ohm measurement systems. PP2 has been fabricated and is currently in test.

It is planned to continue examination of the practical measurement limitations of PP1 on fast rise time pulse modulators. PP2 will be optimized and calibrated during the next reporting period. This will be aided by our recent procurement of two new pieces of equipment, the SPIRE Model 25, 1 kV pulse generator, and the Tektronix Model S-4 sampling head (25 ps rise time).

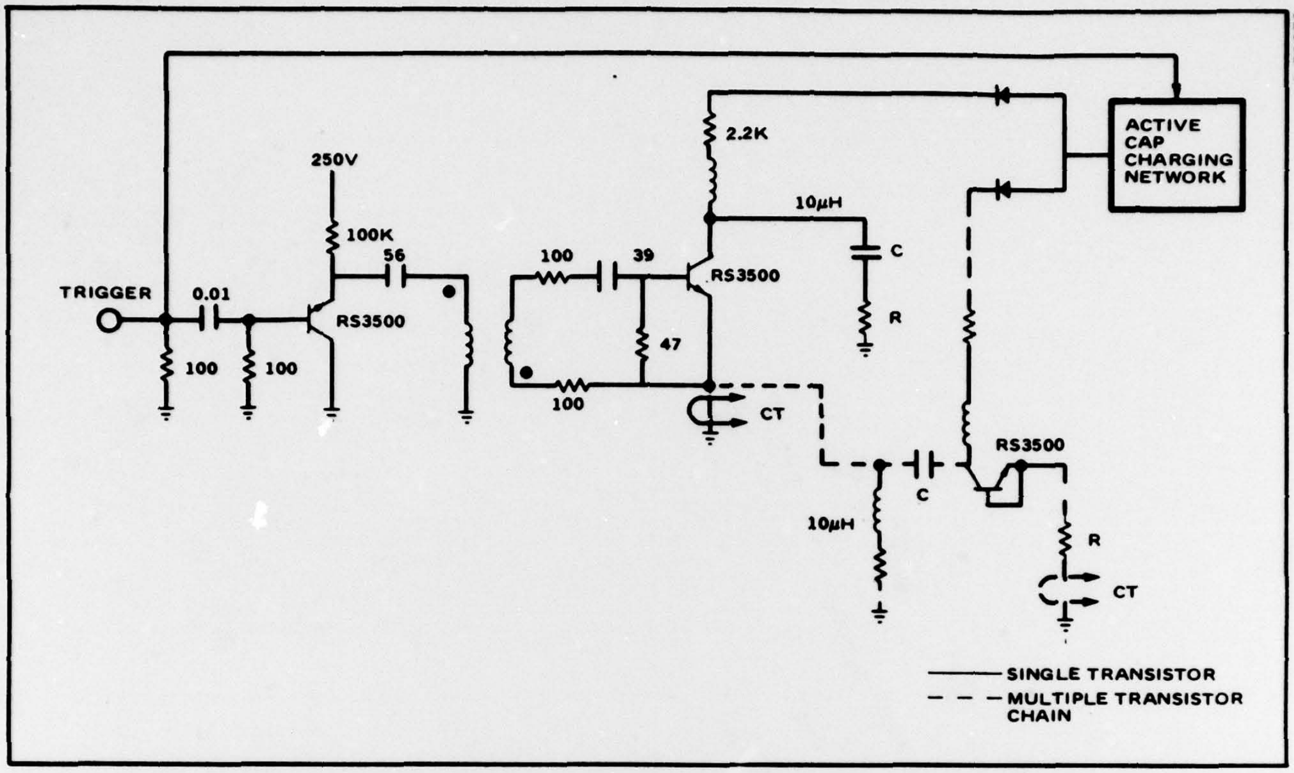
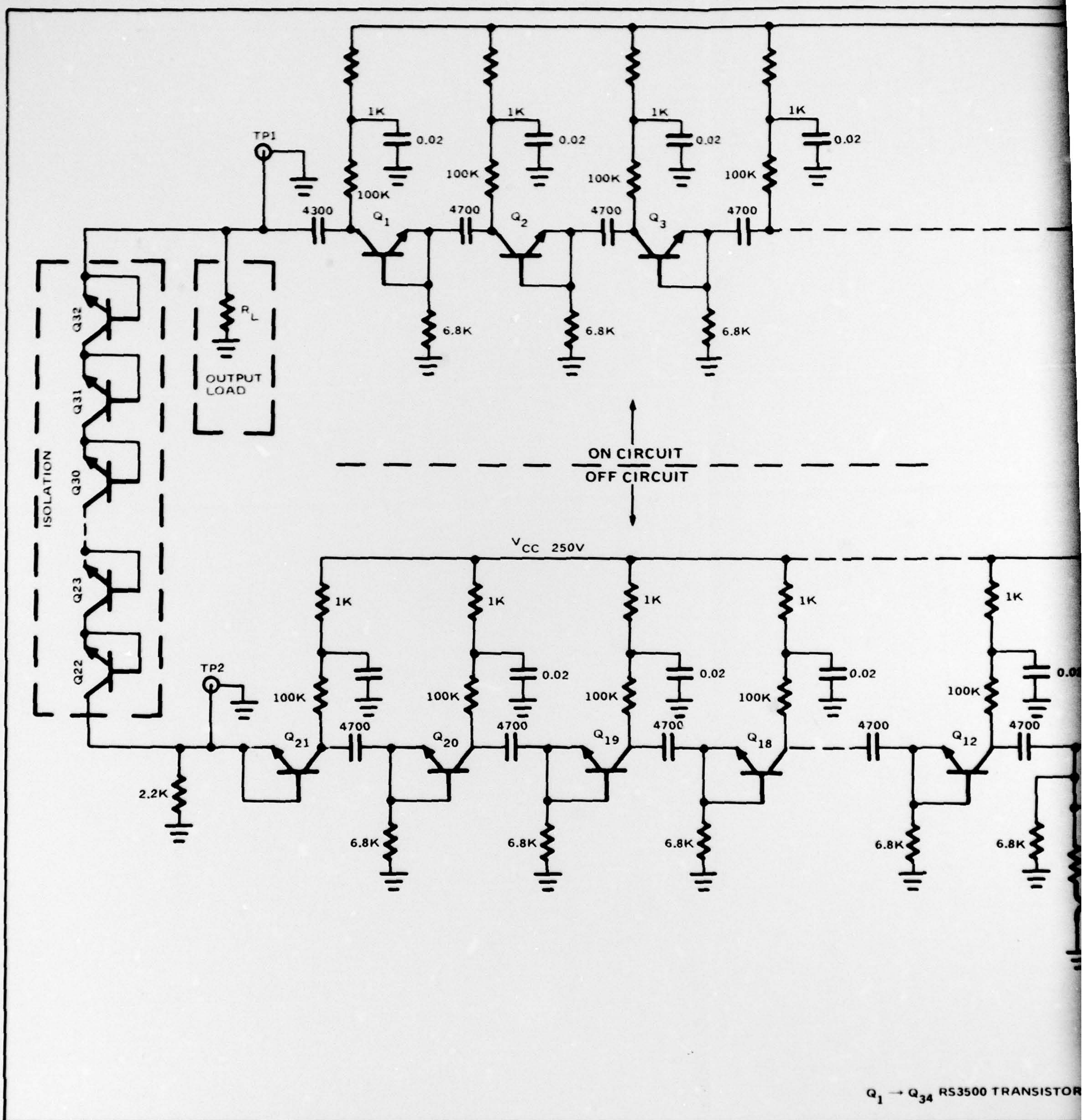


Figure 1. Test Circuit to Evaluate Avalanche Transistor Power Handling Capability



TP1
1K
0.02
100K
4300
4700
Q1
Q2
Q3
6.8K
R L
OUTPUT LOAD
ISOLATION
Q32
Q31
Q30
Q23
Q22
ON CIRCUIT
OFF CIRCUIT
VCC 250V
TP2
2.2K
Q21
Q20
Q19
Q18
Q12
Q1 → Q34 RS3500 TRANSISTOR

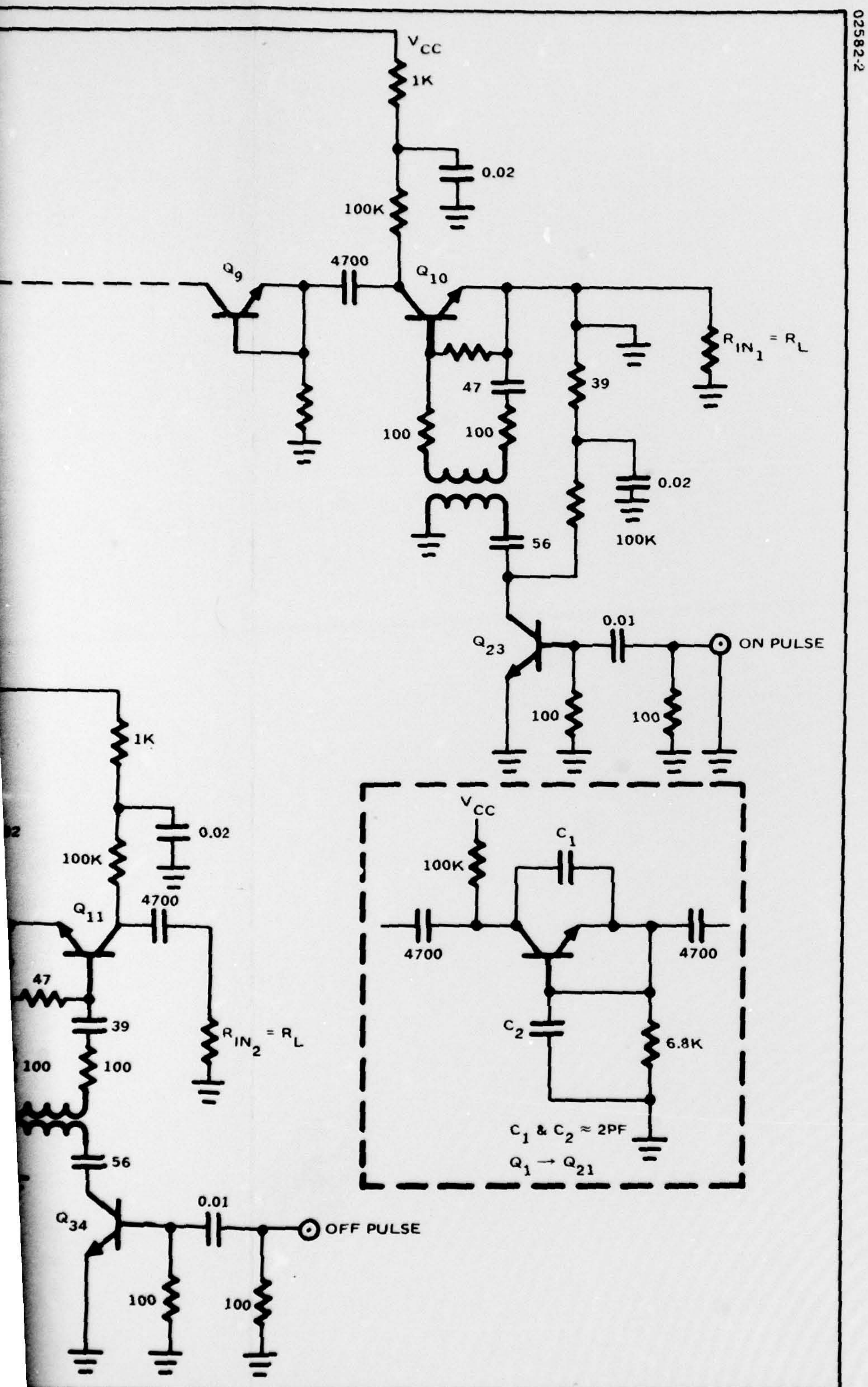
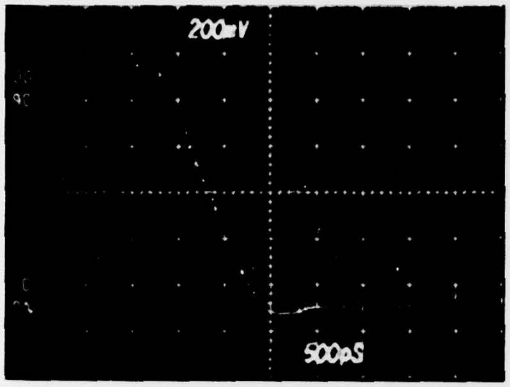
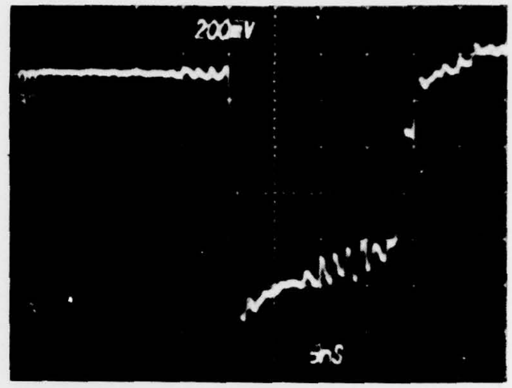


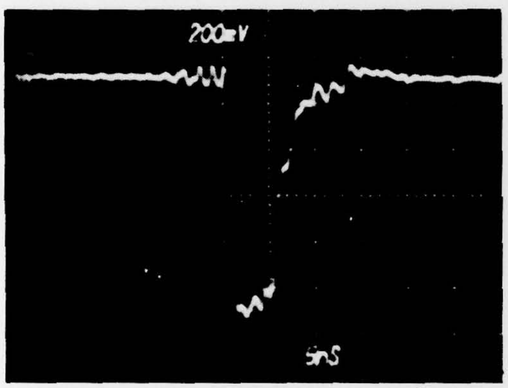
Figure 2. Switch Module Developed for Task A and Task B



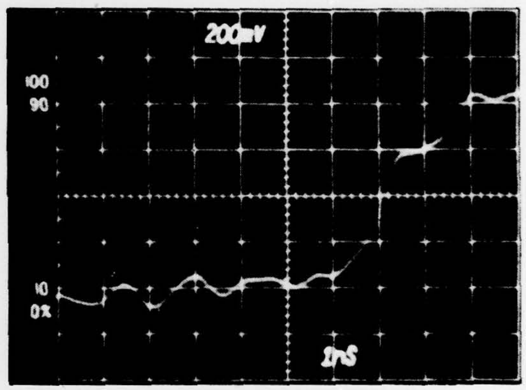
RISETIME
V . . 200 V/cm
H . . 500 ps/cm



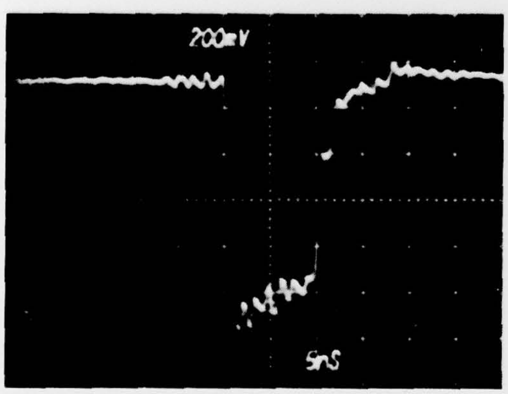
20 ns PULSE
V . . 200 V/cm
H . . 5 ns/cm



5 ns PULSE
V . . 200 V/cm
H . . 5 ns/cm



FALLTIME
V . . 200 V/cm
H . . 1 ns/cm



10 ns PULSE
V . . 200 V/cm
H . . 5 ns/cm

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Figure 3. Pulser Output Waveforms (TP1)

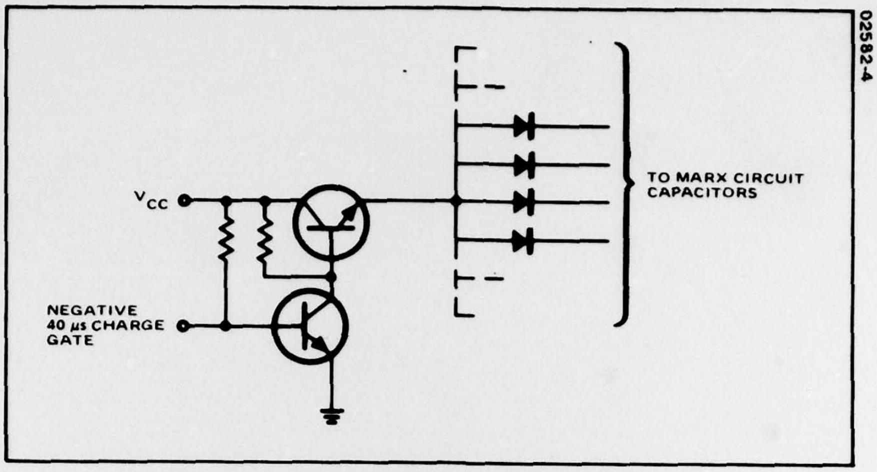

Figure 4. Active Capacitor Charging Circuit

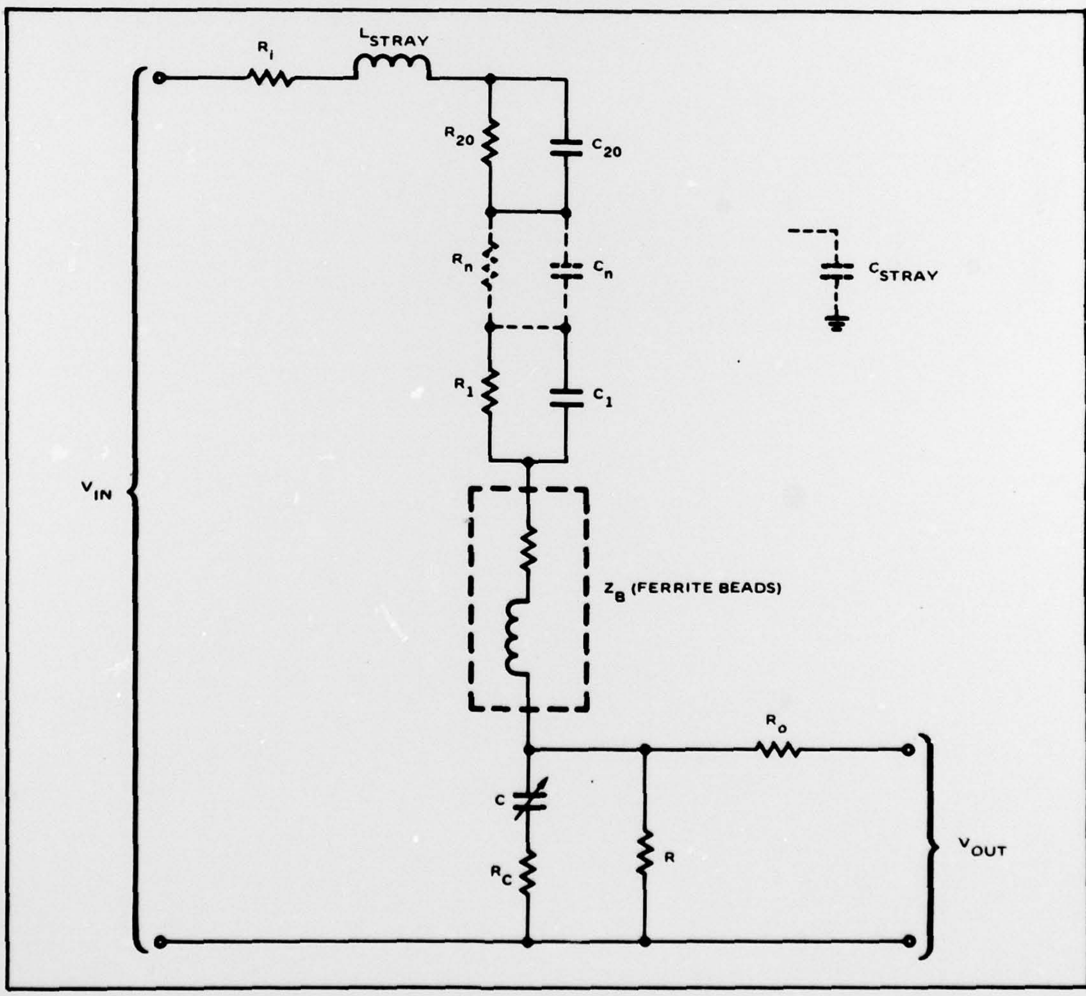

Figure 5. Equivalent Circuit of Probe Prototype 1

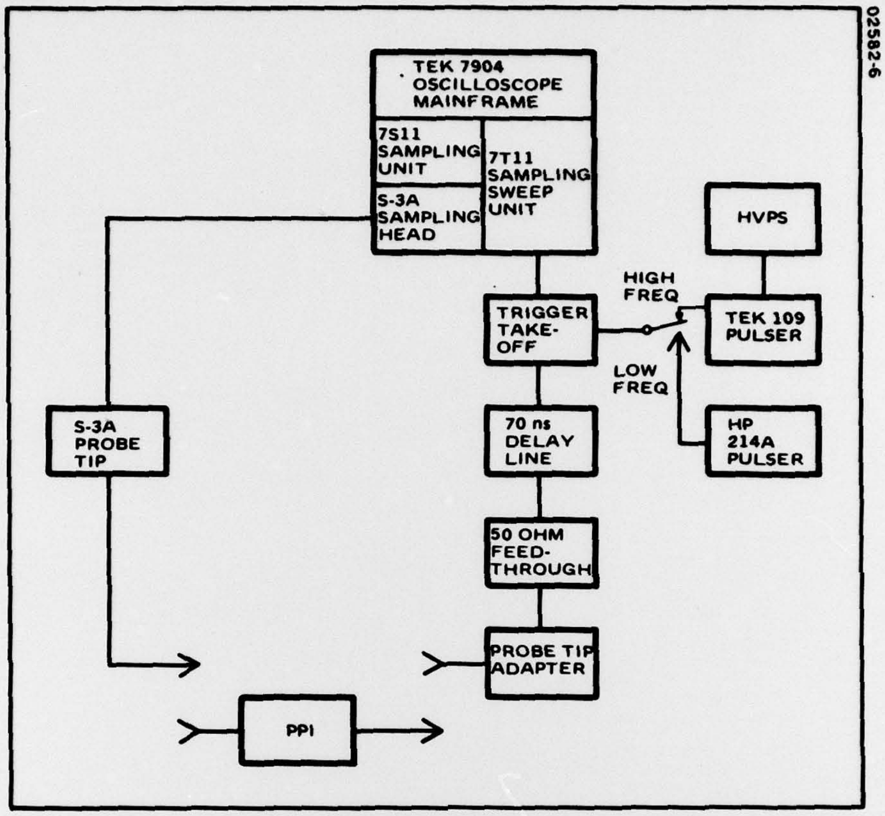

Figure 6. Calibration Test Set-Up

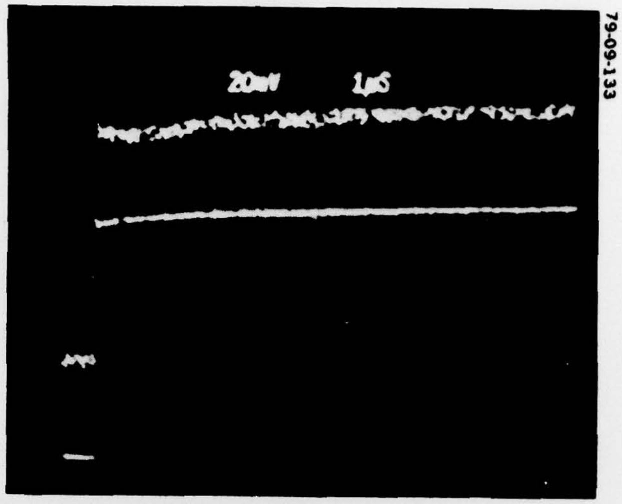

Figure 7. DC Response; Upper Trace, PPI/S-3A at 20 mv/div. Lower trace S-3A alone at 200 mv/div. 1 μs/div sweep.

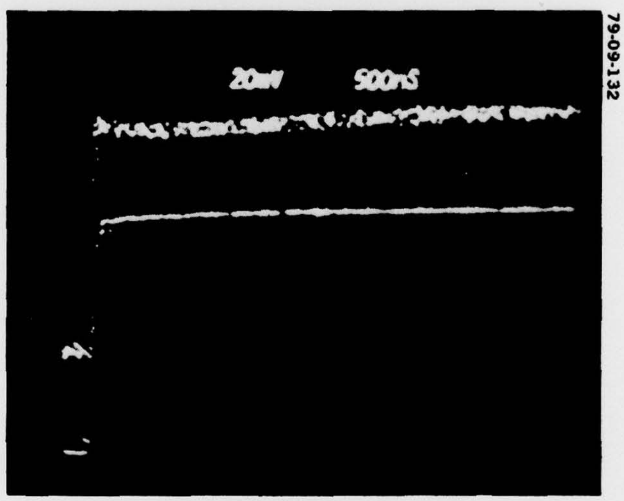

Figure 8. DC Response; Upper Trace, PPI/S-3A at 20 mv/div. Lower trace, S-3A alone at 200 mv/div. 500 ns/div sweep.

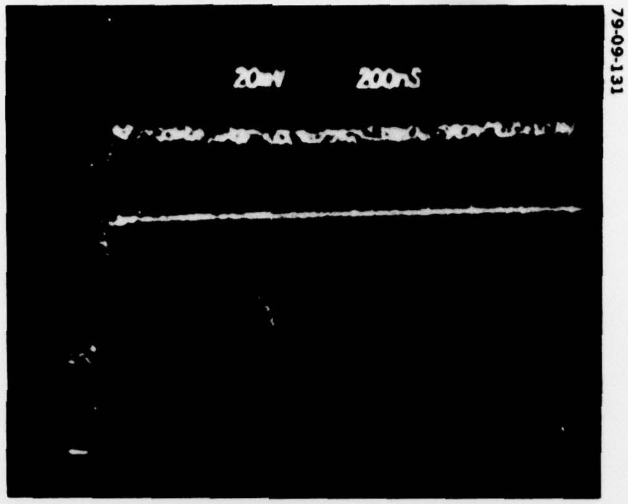

Figure 9. DC Response; Upper Trace PPI/S-3A at 20 mv/div. Lower trace S-3A alone at 200 mv/div sweep.

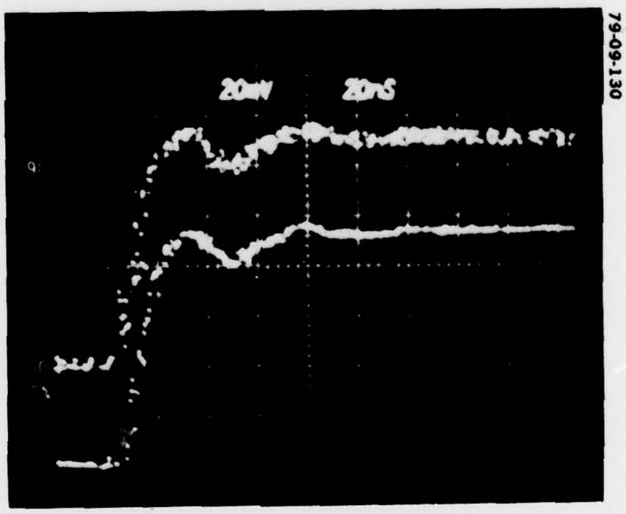

Figure 10. Low Frequency Response; Upper Trace, PPI/S-3A at 20 mv/div. Lower trace, S-3A alone at 200 mv/div, 20 ns/div sweep.

Figure 11. Risetime; S-3A Alone, at 100 ps/div

Figure 12. Risetime; PP1/S-3A, at 100 ps/div

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Figure 13. High Frequency Response; Upper Trace, S-3A Alone. Lower trace, PPI/S-3A with pulse amplitude X10.

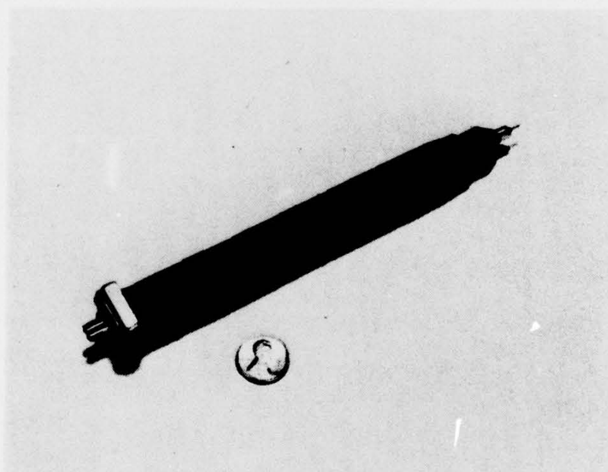

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Figure 14. Probe Prototype 1

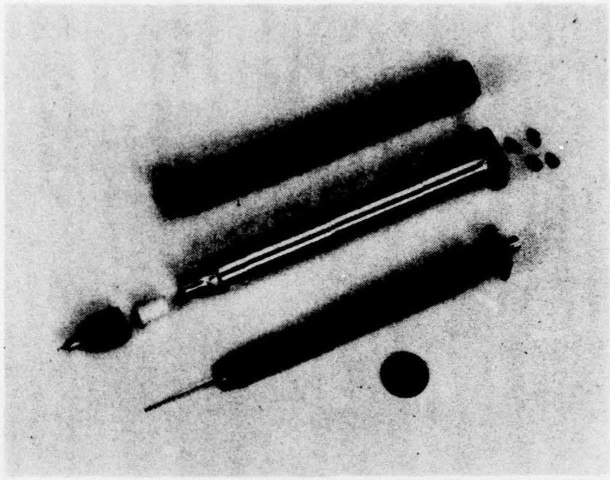

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Figure 15. PPI Parts Breakout

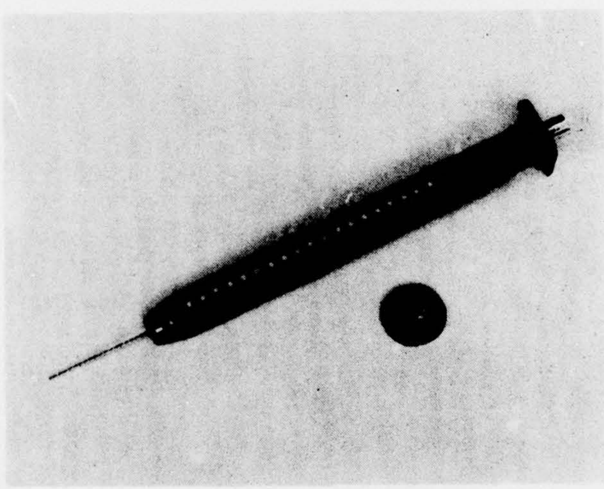

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Figure 16. PPI Circuit Layout

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